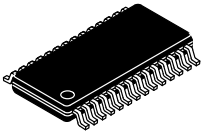
PCS2I2310ANZ

Product Preview

3.3 V SDRAM Buffer for Mobile PCS with 4 SO-DIMMs

ON Semiconductor®

http://onsemi.com



SSOP−28
A SUFFIX
CASE 565AH

Description

The PCS2I2310ANZ is a 3.3 V buffer designed to distribute high−speed clocks in mobile PC applications. The part has 10 outputs, 8 of which can be used to drive up to four SDRAM SO−DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3 V and outputs can run up to 133 MHz, thus making it compatible with Pentium II® processors.

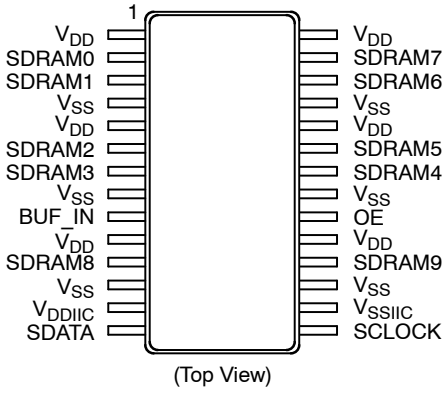
The PCS2I2310ANZ also includes a serial interface (IIC), which can enable or disable each output clock. The IIC is Slave Receiver only and is Standard mode compliant. IIC Master can write into the IIC registers but cannot read back. The first two bytes after address should be ignored by IIC Block and data is valid after these two bytes as given in IIC Byte Flow Table. On power−up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.

Features

- One Input to 10 Output Buffer/Driver
- Supports up to Four SDRAM SO−DIMMs
- Two Additional Outputs for Feedback
- Serial Interface for Output Control
- Low Skew Outputs
- Up to 133 MHz Operation
- Multiple V_{DD} and V_{SS} Pins for Noise Reduction
- Dedicated OE Pin for Testing
- Space−saving 28 Pin SSOP Package
- 3.3 V Operation
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

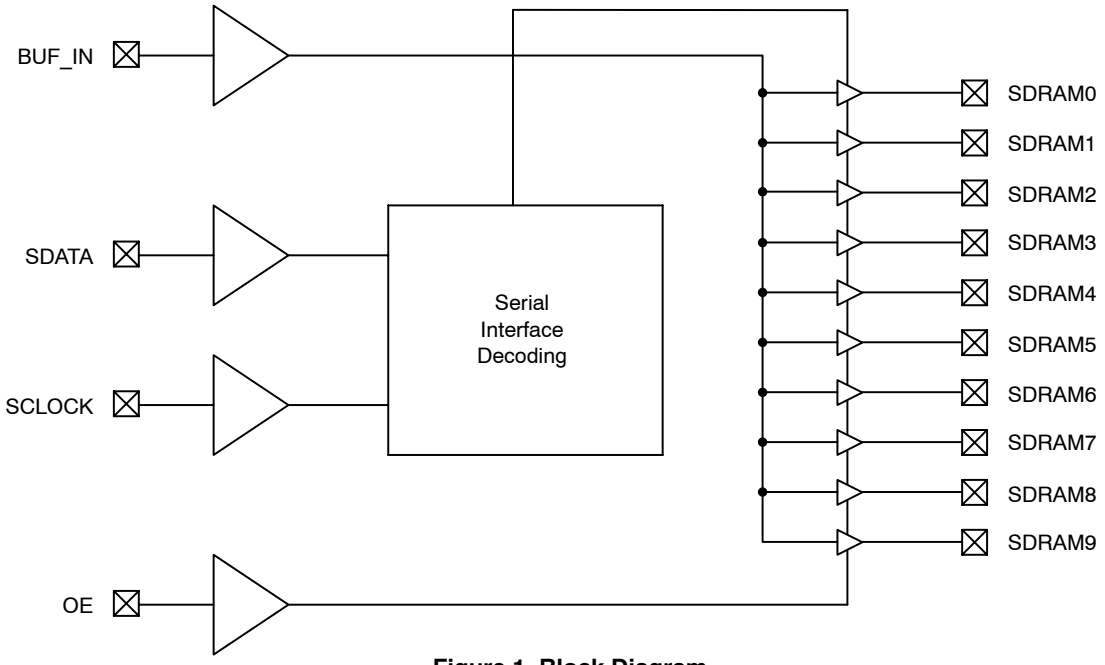


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pins	Name	Type	Description
1, 5, 10, 19, 24, 28	V_{DD}	P	3.3 V Digital voltage supply
4, 8, 12, 17, 21, 25	V_{SS}	P	Ground
13	V_{DDIIC}	P	3.3 V Serial interface voltage supply
16	V_{SSIIC}	P	Ground for serial interface
9	BUF_IN	I	Input clock, 5 V tolerant
20	OE	I	Output Enable, three−states outputs when LOW. Internal pull−up to V_{DD}
14	SDATA	I/O	Bi−directional Serial data pin. Internal pull−up to $V_{DD.}$ 5 V tolerant
15	SCLK	I	Serial clock input. Internal pull−up to $V_{DD.}$ 5 V tolerant
2, 3, 6, 7	SDRAM [0−3]	O	SDRAM byte 0 Clock Outputs
22, 23, 26, 27	SDRAM [4−7]	O	SDRAM byte 1 Clock Outputs
11, 18	SDRAM [8−9]	O	SDRAM byte 2 Clock Outputs

Table 2. DEVICE FUNCTIONALITY

OE	SDRAM [0–17]
0	High−Z
1	1 x BUF_IN

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:
  1. Byte 0 − Bits 7, 6, 5, 4, 3, 2, 1, 0
  2. Byte 1 − Bits 7, 6, 5, 4, 3, 2, 1, 0
  3. Byte N − Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits can be programmed to either “0” or “1”.
- Serial interface address for the PCS2I2310ANZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	−−−

Table 3. BYTE 0: SDRAM Active/Inactive Register
(Note 1) (1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	−−	Unused
Bit 6	−−	Unused
Bit 5	−−	Unused
Bit 4	−−	Unused
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

Table 4. BYTE 1: SDRAM Active/Inactive Register
(Note 1) (1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	27	SDRAM7 (Active/Inactive)
Bit 6	26	SDRAM6 (Active/Inactive)
Bit 5	23	SDRAM5 (Active/Inactive)
Bit 4	22	SDRAM4 (Active/Inactive)
Bit 3	−−	Unused
Bit 2	−−	Unused
Bit 1	−−	Unused
Bit 0	−−	Unused

Table 5. BYTE 2: SDRAM Active/Inactive Register
(Note 1) (1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	18	SDRAM9 (Active/Inactive)
Bit 6	11	SDRAM8 (Active/Inactive)
Bit 5	−−	Reserved
Bit 4	−−	Reserved
Bit 3	−−	Reserved
Bit 2	−−	Reserved
Bit 1	−−	Reserved
Bit 0	−−	Reserved

Table 6. IIC BYTE FLOW

Byte	Description
1	IIC Address
2	Command (dummy value, ignored)
3	Byte Count (dummy value, ignored)
4	IIC Data Byte 0
5	IIC Data Byte 1
6	IIC Data Byte 2

1. When the value of bit in these bytes is high, the output is enabled. When the value of the bit is low, the output is forced to low state. The default value of all the bits is high after chip is powered up.

Table 7. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage to Ground Potential	−0.5 V to +7.0	V
V_{IN}	DC Input Voltage (Except BUF_IN)	−0.5 V to V_{DD} + 0.5	V
V_{INB}	DC Input Voltage (BUF_IN)	−0.5 V to +7.0	V
T_{STG}	Storage Temperature	−65°C to +150	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 8. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance	20	30	pF
C_{IN}	Input Capacitance		7	pF
t_{PU}	Power−up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Table 9. ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage	Except serial interface pins			0.8	V
V_{ILIIC}	Input LOW Voltage	For serial interface pins only			0.7	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{OL}	Output LOW Voltage (Note 2)	I_{OL} = 25 mA			0.4	V
V_{OH}	Output HIGH Voltage (Note 2)	I_{OH} = −36 mA	2.4			V
I_{CC}	Quiescent Supply Current	V_{DD} = 3.465 V, V_i = V_{DD} or GND, I_O = 0		50	100	μA
I_{OZ}	High Impedance Output Current	V_{DD} = 3.465 V, V_i = V_{DD} or GND			±10	μA
I_{OFF}	OffState Current (for SCL ,SDATA)	V_{DD} = 0 V, V_i = 0 V or 5.5 V			50	μA
ΔI_{CC}	Change in Supply Current	V_{DD} = 3.135 V to 3.465 V One Input at V_{DD} − 0.6, All other Inputs at V_{DD} or GND			500	μA
I_i	Input Leakage	V_{DD} = 3.465 V or GND (Applicable to all Input Pins)	−5		+5	μA
I_{DD}	Supply Current (Note 2)	Unloaded outputs, 133 MHz			266	mA
I_{DD}	Supply Current (Note 2)	Loaded outputs, 30 pF, 133 MHz			360	mA
I_{DD}	Supply Current (Note 2)	Unloaded outputs, 100 MHz			200	mA
I_{DD}	Supply Current (Note 2)	Loaded outputs, 30 pF, 100 MHz			290	mA
I_{DD}	Supply Current (Note 2)	Unloaded outputs, 66.67 MHz			150	mA
I_{DD}	Supply Current (Note 2)	Loaded outputs, 30 pF, 66.67 MHz			185	mA
I_{DDS}	Supply Current	BUF_IN = V_{DD} or V_{SS}, all other inputs at V_{DD}			500	μA

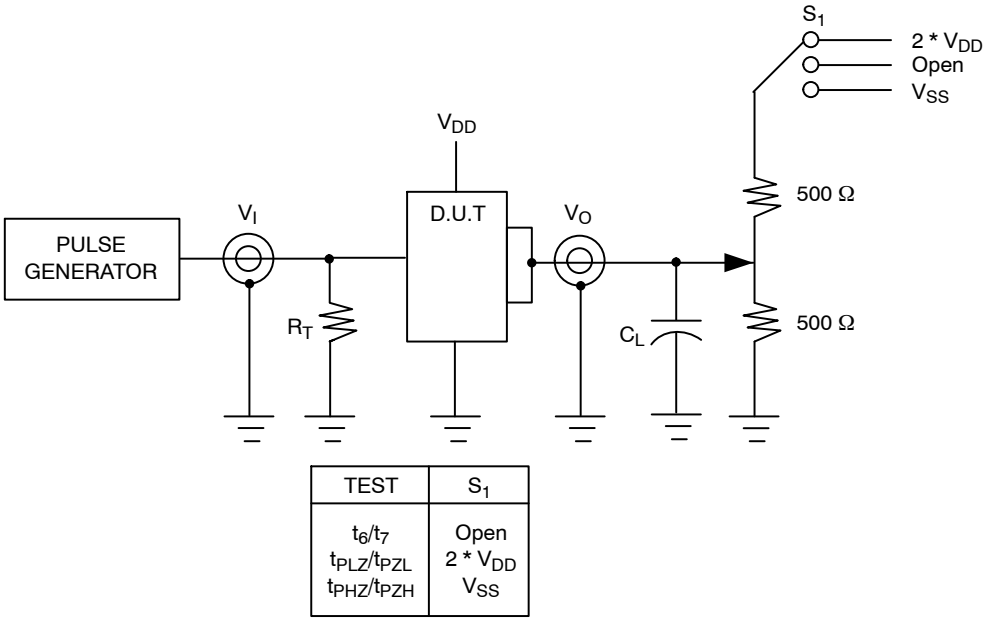
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 10. SWITCHING CHARACTERISTICS (Note 3)

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
f_{max}	Maximum Operating Frequency				133	MHz
t_D	Duty Cycle (Notes 4, 5) = $t_2 \div t_1$	Measured at 1.5 V	45.0	50.0	55.0	%
t_3	Rising Edge Rate (Note 5)	Measured between 0.4 V and 2.4 V	1	2	4	V/nS
t_4	Falling Edge Rate (Note 5)	Measured between 2.4 V and 0.4 V	1	2	4	V/nS
t_5	Output−to−Output Skew (Note 5)	All outputs equally loaded		150	225	pS
t_6	SDRAM Buffer LH Prop. Delay (Note 5)	Input edge greater than 1 V/nS	1	2.7	3.5	nS
t_7	SDRAM Buffer HL Prop. Delay (Note 5)	Input edge greater than 1 V/nS	1	2.7	3.5	nS
t_{PLZ}, t_{PHZ}	SDRAM Buffer Enable Delay (Note 5)	Input edge greater than 1 V/nS	1	3	5	nS
t_{PZL}, t_{PZH}	SDRAM Buffer Disable Delay (Note 5)	Input edge greater than 1 V/nS	1	3	5	nS
t_r	Rise Time for SDATA (Refer to *Test Circuit for IIC*) Refer to *Figure 4*	C_L = 10 pF	6			nS
		C_L = 40 pF			250	
t_f	Fall Time for SDATA (Refer to *Test Circuit for IIC*) Refer to *Figure 4*	C_L = 10 pF	20			nS
		C_L = 40 pF			250	

3. All parameters specified with loaded outputs.
4. Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1 V/nS.
5. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Test Circuit for SDRAM Enable and Disable Times



TEST	S_1
t_6/t_7	Open
t_{PLZ}/t_{PZL}	2 * V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}

Figure 2. Load Circuit for Switching Times

SDRAM Enable and Disable Times

V_M = 1.5 V
$V_X = V_{OL}$ + 0.3 V
$V_Y = V_{OH}$ − 0.3 V
V_{OH} and V_{OL} are the typical Output Voltage drop that occur with the output load.

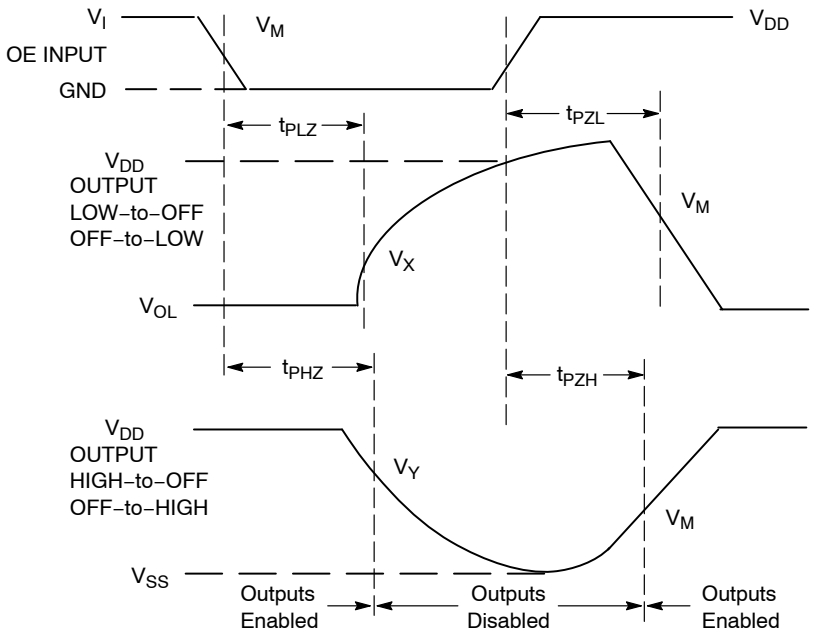


Figure 3. State Enable and Disable Times

Test Circuit for IIC Rise and Fall Times

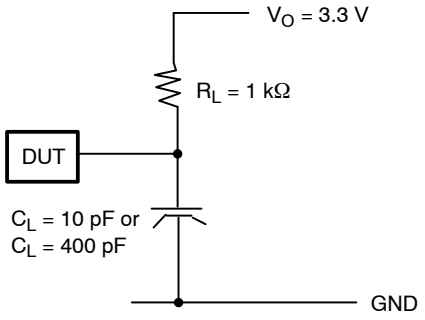


Figure 4. Test Circuit for IIC

Switching Waveforms

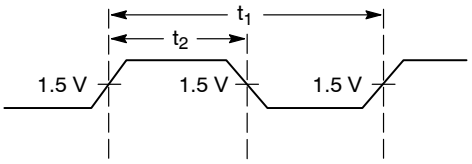


Figure 5. Duty Cycle Timing

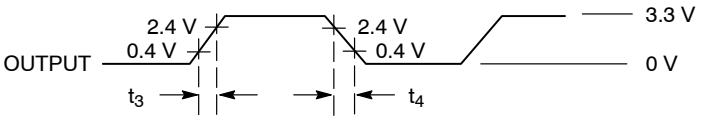


Figure 6. All Outputs Rise/Fall Time

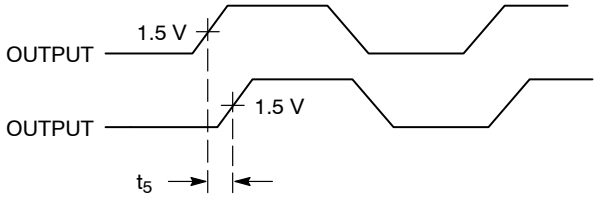


Figure 7. Output−Output Skew

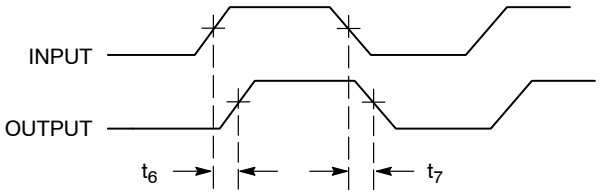


Figure 8. SDRAM Buffer LH and HL Propagation Delay

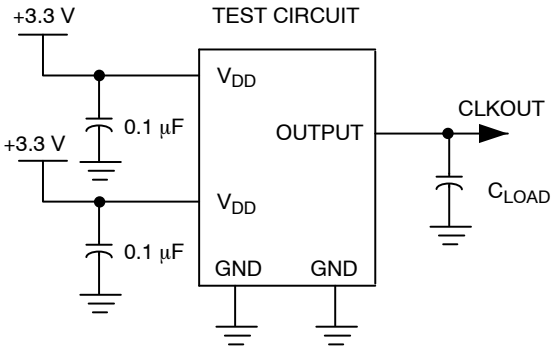


Figure 9. Test Circuits

Application Information

Clock traces must be terminated with either series or parallel termination, as is normally done.

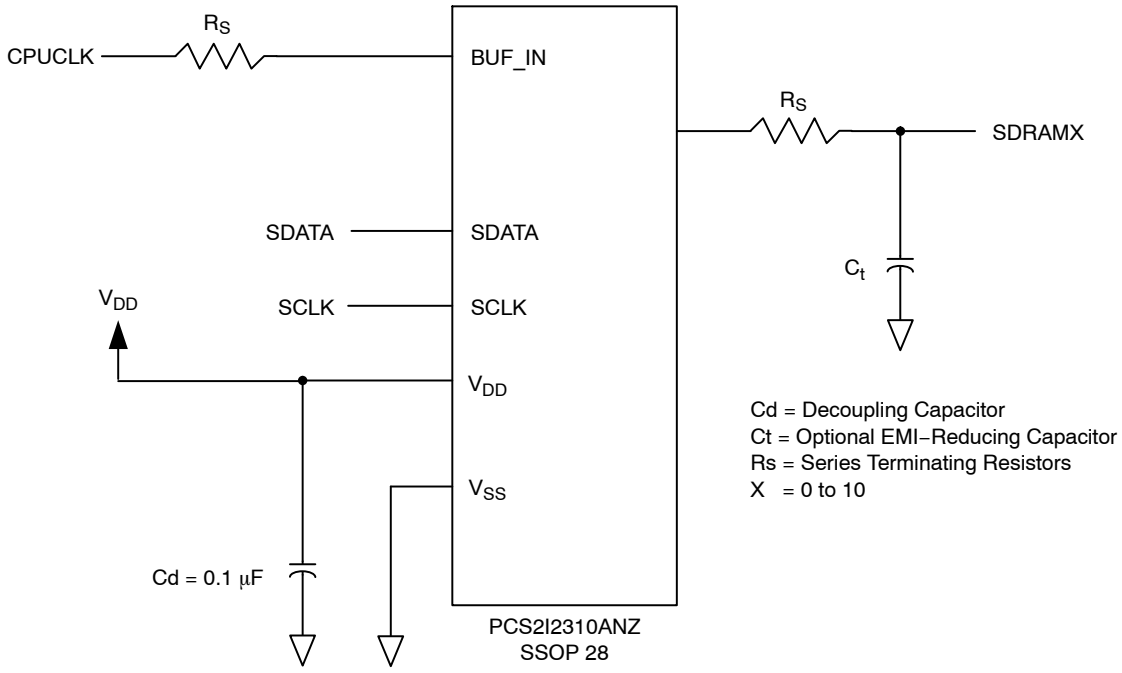


Figure 10.

Summary

- Surface mount, low−ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where Rtrace is the loaded characteristic impedance of the trace, Rout is the output impedance of the buffer (typically 25 Ω), and Rseries is the series terminating resistor.

  Rseries > Rtrace – Rout
- Footprints must be laid out for optional EMI−reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.
- A Ferrite Bead may be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50 Ω impedance at the clock frequency, under loaded DC conditions.
- If a Ferrite Bead is used, a 10 μF–22 μF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

IIC Serial Interface Information

The information in this section assumes familiarity with IIC programming.

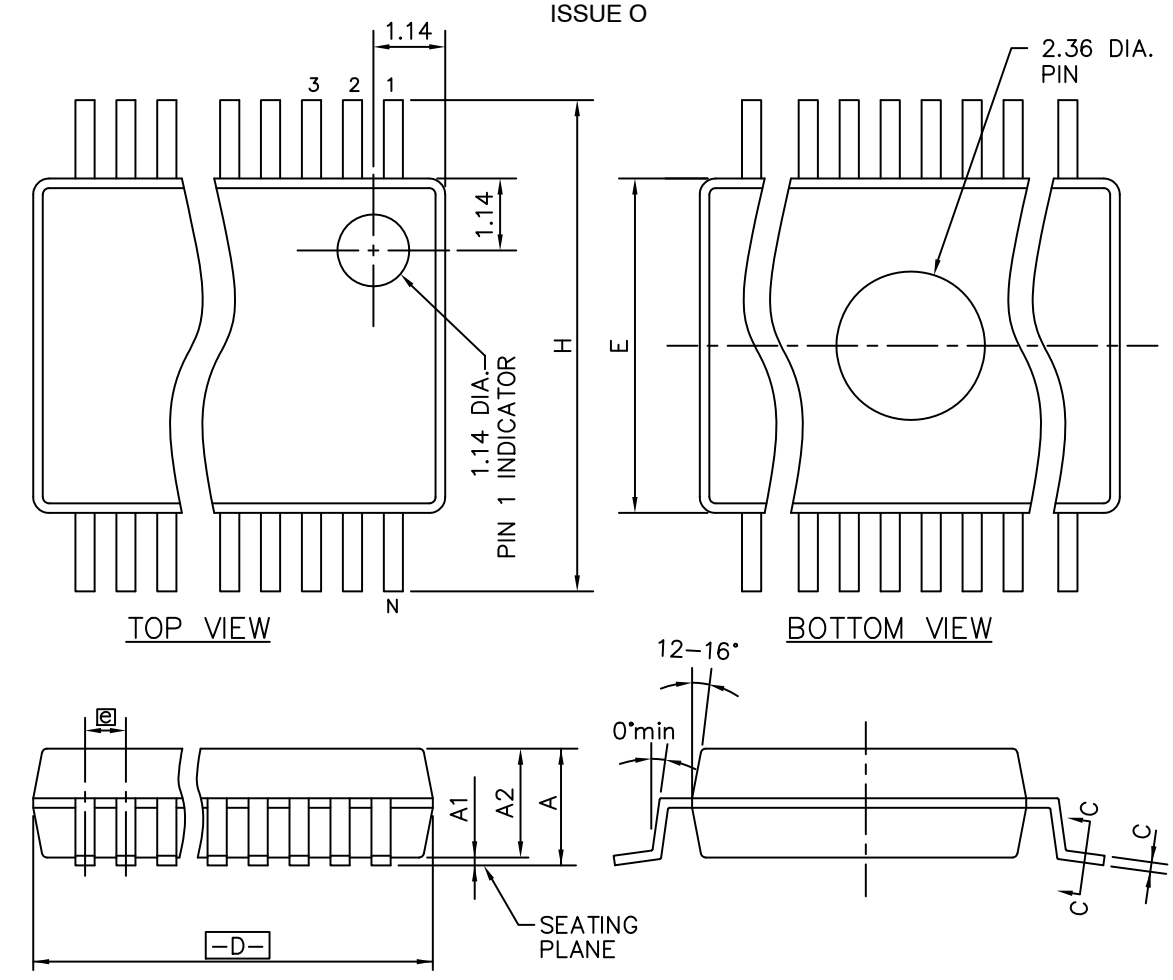
How to Program PCS2I2310ANZ through IIC:

- Master (host) sends a start bit.
- Master (host) sends the write address D3 (H).
- PCS2I2310ANZ device will acknowledge.
- Master (host) sends the Command Byte.
- PCS2I2310ANZ device will acknowledge the Command Byte.
- Master (host) sends a Byte count.
- PCS2I2310ANZ device will acknowledge the Byte count.
- Master (host) sends the Byte 0.
- PCS2I2310ANZ device will acknowledge Byte 0.
- Master (host) sends the Byte 1.
- PCS2I2310ANZ device will acknowledge Byte 1.
- Master (host) sends the Byte 2.
- PCS2I2310ANZ device will acknowledge Byte 2.
- Master (host) sends a Stop bit.

Controller (Host)	PCS2I2310ANZ (slave/receiver)
Start Bit	
Slave Address D3(H)	
	ACK
Command Byte	
	ACK
Byte count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Stop Bit	

PACKAGE DIMENSIONS

SSOP 28
CASE 565AH−01
ISSUE O



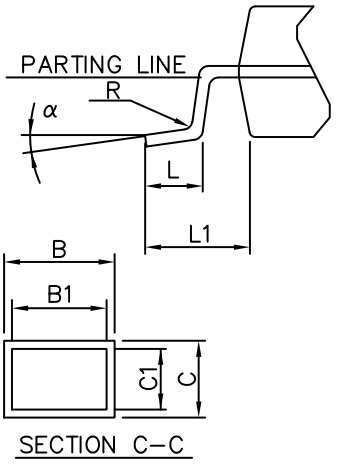


TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	1			2
					VARI−	D			N
	MIN.	NOM.	MAX.		ATIONS	MIN.	NOM.	MAX.	
A	1.73	1.86	1.99			2.87	3.00	3.13	8
A_1	0.05	0.13	0.21		AA	6.07	6.20	6.33	14
A_2	1.68	1.73	1.78		AB	6.07	6.20	6.33	16
B	0.25	−	0.38		AC	7.07	7.20	7.33	20
B1	0.25	0.30	0.33		AD	8.07	8.20	8.33	24
C	0.09	−	0.20		AE	10.07	10.20	10.33	28
C1	0.09	0.15	0.16		AF	10.07	10.20	10.33	30
D	SEE VARIATIONS			1					
E	5.20	5.30	5.38						
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95						
L1	1.25 REF.								
N	SEE VARIATIONS			2					
α	0°	4°	8°						
R	0.09	0.15	−						

NOTE:
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm on D PER SIDE.

Table 11. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
PCS2P2310ANZG−28−AT	2P2310ANZG	28−pin SSOP −Tube, Green	Commercial
PCS2P2310ANZG−28−AR	2P2310ANZG	28−pin SSOP −Tape and Reel, Green	Commercial
PCS2I2310ANZG−28−AT	2I2310ANZG	28−pin SSOP −Tube, Green	Industrial
P2I2310ANZG−28AR	2I2310ANZG	28−pin SSOP −Tape and Reel, Green	Industrial

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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P.O. Box 5163, Denver, Colorado 80217 USA
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